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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,716	10/27/2003	Kouta Yasunaga	61282-042	9704

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EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,716	YASUNAGA, KOUTA	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on January 17, 2006. Claims 1-5 have been amended. Claims 6-10 are newly added. Claims 1-10 are presented for examination. Claims 1-10 are pending.

The information disclosure statement (IDS) submitted on February 9, 2006 was filed after the mailing date of the Amendment on January 17, 2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Applicant's Amendment filed January 17, 2006 has been fully considered and the rejections are maintained as follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sharma et al. (US 6,108,737).

As per claim 1, Sharma et al. disclosed a shared memory data transfer apparatus (see Fig. 1), where a plurality of masters (see Fig. 1, items 102-108, col. 5, lines 48-50)

access one shared memory (see Fig. 1, item 150, col. 5, lines 50-55) to perform data transfers, the disclosed shared memory apparatus comprising:

a plurality of master interface circuits (see Fig. 2, items 202-208, col. 7, lines 44-46) respectively connected to the masters **102-108.**

a plurality of write buffers (see Fig. 2, items 222-230, col. 7, lines 50-51) respectively connected to the master interface circuits **202-208** for retaining data written from said masters **102-108** to said shared memory **150**,

a plurality of read buffers (see Fig. 2, items 212-220, col. 7, lines 49-50) respectively connected to the master interface circuits **202-208** for retaining data read from said shared memory **150** to said masters **102-108**.

a FIFO (see Fig. 5, items 522-536, col. 11, lines 13-15, and lines 41-45) coupled to said plurality of master interface circuits **202-208**, and operable for receiving commands from said master interface circuits (col. 11, lines 13-15, and lines 41-45) for storing commands in a first-in, first-out manner (see col. 15, lines 7-10, *which will further enforce the previous citation*), and

a shared memory interface circuits (see Fig. 2, item 170, col. 6, lines 59-62) for controlling data transfers from the write buffers **222-230** (see col. 7, lines 48-49, *which further enforce the previous citation*) to said shared memory or data transfers from the shared memory **150** to the read butters **212-220** (see col. 7, lines 49-50, *which further enforce the previous citation*) in accordance with commands fetched from the FIFO **522-536** (see col. 15, lines 7-10, *which further enforce the previous citation*)

As per claim 2, Sharma et al. disclosed a shared memory data transfer apparatus (Fig. 1) further comprising an arbiter (see Fig. 2, item 240) for storing/receiving a plurality of simultaneously issued commands into the FIFO (input queue) in a predetermined order (col. 7, lines 53-55).

As per claim 3 Sharma et al. disclosed a shared memory apparatus (Fig. 1) further comprising an arbiter (see Fig. 2, item 240) for referencing the command contents and rearranging the order of commands to be stored into the FIFO (input queue) (col. 7, lines 53-67, col. 11, lines 13-15, and lines 41-45).

As per claims, 4, 6, and 7, Sharma et al. disclosed a shared memory data transfer apparatus which issues command to be stored into said FIFO per access to said shared memory (col. 11, lines 13-15 and lines 41-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (U.S. Patent 6108737) in view of Phelan (U.S. Patent 6651134).

As per claims 5 and 8-10, Sharma et al. failed to disclose a shared memory data transfer apparatus, which uses a fixed burst length in an access to said shared memory.

Phelan disclosed a fixed burst length in an access of a memory. See col. 3, lines 41-47. It would have been obvious to one having ordinary skill in the art at the time of the Applicant's invention to realize that it is advantageous to modify the system of Sharma et al. to combine with the system of Phelan since having a fixed burst length it may aid the circuit to operate at higher frequency while avoiding data refreshing as taught by Phelan on col. 3, lines 41-43.

Response to Arguments

Applicant's arguments filed January 17, 2006 have been fully considered but they are not persuasive.

In respond to the Applicant counsel's remarks:

Applicant counsel argued in respect to claim 1 that Sharma et al. failed to disclose or suggest:

(a) the master interface circuits (page 6, third paragraph, lines 1-2).

(b) the shared memory interface circuit (page 6, third paragraph, lines 1-2; page 7, first paragraph, lines 1-2).

(c) the use of FIFO in the embodiments shown in Figs. 1 and 2 of Sharma et al. (page 6, first paragraph, lines 2-3, lines 8-9).

(d) a shared memory interface circuit coupled to the FIFO (page 7, first paragraph, lines 3-4).

With respect to (a) and (b):

Examiner respectfully disagree with the remarks indicating that Sharma et al. failed to disclose or suggest the master interface circuits and shared memory interface circuits. Fig. 2, items 202- 208 and col. 7, lines 44-46 suggest that there is a form communication between the local switch 200 with each of the master (col. 7, lines 60-63). Therefore, a master interface circuit must be existed in the system of Sharma et al. order to enable the communication mean between the master and the switch.

Furthermore, shared memory interface circuit also has to be existed in order to communicate between the shared memory 150 with the arbiter 240 through the bus 170 as shown in Fig. 2 and further disclosed in col. 7, lines 53-55.

With respect to (c):

Further review indicates that, however, the FIFO is not shown in Fig. 1 and 2 of Sharma et al. but it is shown in Fig. 5 of Sharma et al. (see claim 1 rejection); wherein the hierarchical switch 500 in Fig. 5 is connected with multiple nodes (see Fig. 14 for a broader representation of Sharma et al. invention). In Fig. 14, the hierarchical switch 1450 is coupled to each and every node and further coupled to a local switch (Fig. 2, item 200) of each node (See col. 10, line 66 – col. 11, line 7 for further clarification). Since each master interface circuit is coupled to the local switch 200 and the local switch 200 further coupled to the hierarchical switch 1450, wherein hierarchical switch 1450 comprises of a FIFO (Fig. 5, items 522-536). Therefore, a FIFO is also coupled to the master interface circuits for storing commands sending from each node in first-in, first-out manner (col. 11, lines 13-15, and 41-45). And each command is apparently

generated from each master of each node and transmitted through the master interface circuit. In conclusion, the limitation: "a FIFO coupled to said plurality of master interface circuits, and operable for receiving commands from said master interface circuits and for storing commands in a first-in, first out manner" of claim 1 is clearly anticipated by the disclosure of Sharma et al.

With respect to (d):

For the same reason from (c), Fig. 2 is an individual node that comprises of masters, master interface circuits, buffers, shared memory, and shared memory interfaces coupled together as a node. Fig. 14 is representing a multiprocessing system with multiple nodes coupled a hierarchical switch 1450. Fig. 5 further defined the hierarchical switch that comprises of a FIFO command queue (col. 11, lines 13-15, and 41-45). Since the shared memory interface circuit is coupled to the local switch 200 and the local switch 200 further coupled to the hierarchical switch 1450, wherein the hierarchical switch 1450 comprises of a FIFO command queue that coupled to the hierarchical switch. Therefore, a FIFO is also coupled to the shared memory interface circuit.

With respect to Applicant counsel's argument regarding the different embodiment of between Fig. 1 & 2 and Fig. 5 of Sharma et al. (page 6, 2nd paragraph, lines 3-4):

Applicant counsel suggests that the hierarchical switch 500 illustrated in Fig. 4 of Sharma et al. does not appear to be able to be utilized in the embodiments shown in Figs. 1 & 2. Examiner respectfully disagree. As discussed from (c) and (d) above, it

clearly proved that the hierarchical switch 500 is being utilized and sharing the functionalities of a FIFO in the hierarchical switch 500.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

VanDoren et al. (hereinafter VanDoren) of U.S Patent 6,122,714, which is incorporated into the invention of Sharma et al. as stated in col. 11, lines 22-24. In that disclosure of '714, VanDoren teaches a plurality of SIB (Fig. 3, items 25a-e) that comprise of plurality of FIFO buffer (Fig. 4A, items 32a-h, col. 9, lines 54-55). Wherein, as discloses in Fig. 3, the system of VanDoren also comprises of masters (P0-P3), an arbiter (27), shared memory (13a-13d), and read and write buffers (Fig. 4A, 32a-3h).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh Vo
Patent Examiner
Art Unit: 2189
3/30/2006

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER